

CLAIMS

Thus, having described the systems and methods for identifying solder joint defects, I claim the following:

1 1. A method for adapting test thresholds, comprising the following steps:
 2 acquiring location information for a plurality of solder joints on a printed-circuit
 3 device;
 4 obtaining information indicative of the variation in distance between a mounting
 5 surface of the printed-circuit device and a printed-circuit board;
 6 recording a measurement of a physical property of a plurality of solder joints used to
 7 couple the printed-circuit device to the printed-circuit board;
 8 estimating a range of acceptable measurements for respective solder joints responsive
 9 to variation in distance between the mounting surface of the printed-circuit device and the
 10 printed-circuit board; and
 11 setting at least one threshold responsive to the range.

1 2. The method of claim 1, wherein the step of acquiring location information
 2 comprises an investigation of an array package.

1 3. The method of claim 1, wherein the step of recording comprises a diameter
 2 measurement.

1 4. The method of claim 1, wherein the step of recording comprises a height
 2 measurement.

1 5. The method of claim 1, wherein the step of recording comprises a volume
 2 measurement.

1 6. The method of claim 1, wherein the estimating step comprises performing a
 2 statistical analysis on recorded measurements of an identified set of neighbor solder joints.

1 7. The method of claim 6, wherein the statistical analysis comprises calculating
2 the median of the recorded measurements of the identified set of neighbor solder joints.

1 8. The method of claim 1, wherein the estimating step comprises formulating a
2 best fit polynomial equation using the recorded measurements of a plurality of solder joints.

1 9. The method of claim 1, wherein the estimating step comprises applying the
2 recorded measurements of a plurality of solder joints in a Fourier analysis.

1 10. The method of claim 9, wherein the Fourier analysis comprises the application
2 of a high-frequency filter on the recorded measurements of an identified set of solder joints
3 distributed across the surface of the device.

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1 14. A method for identifying solder joint defects, comprising the steps of:
2 recording a measurement associated with a plurality of solder joints on a printed-
3 circuit device;
4 estimating an expected value for the plurality of solder joints that accounts for
5 acceptable variance in the distance between the mounting surfaces of a printed-circuit device
6 and a printed-circuit board coupled by the solder joints;
7 comparing the recorded measurement with the expected value for the plurality of
8 solder joints to generate a respective error value; and
9 identifying defective solder joints by applying an error value outlier analysis to the
10 plurality of error values.

15. The method of claim 14, wherein the step of recording comprises an
investigation of an array package.

16. The method of claim 14, wherein the step of recording comprises a diameter
measurement.

17. The method of claim 14, wherein the step of estimating an expected value for
the plurality of solder joints comprises performing a statistical analysis on the recorded
measurements of a set of neighboring solder joints.

18. The method of claim 14, wherein the step of estimating an expected value for
the plurality of solder joints comprises performing a statistical analysis on the recorded
measurements of a set of solder joints equidistant from the centroid of the printed-circuit
device.

19. The method of claim 17, wherein the statistical analysis comprises calculating
the median of the recorded measurements of the identified set of neighboring solder joints.

20. The method of claim 14, wherein the step of estimating an expected value for
respective solder joints comprises formulating a best fit polynomial equation using the
recorded measurements of the plurality of solder joints.

1 21. The method of claim 14, wherein the step of estimating an expected value for
2 the plurality of solder joints comprises applying the recorded measurements of a plurality of
3 solder joints in a Fourier analysis.

1 22. The method of claim 21, wherein the Fourier analysis comprises the
2 application of a high-frequency filter on the recorded measurements of a plurality of solder
3 joints.

1 23. The method of claim 14, wherein the step of comparing the expected value
2 with the recorded measurement comprises a mathematical combination of the expected value
3 with the respective recorded measurement.

24. The method of claim 23, wherein the mathematical combination comprises the
difference of the expected value with the respective recorded measurement.

25. The method of claim 23, wherein the step of identifying defective solder joints
comprises a box plot analysis responsive to the plurality of error values.

26. An improved solder-joint inspection system, comprising:
means for measuring at least one characteristic of a plurality of solder joints on a
printed-circuit device;
means for computing an expected value for the measured characteristic for each of the
plurality of solder joints that varies as a function of distance between the mounting surface of
the printed-circuit device and a printed-circuit board; and
means for formulating an error value as a function of the measured characteristic and
the expected value for the plurality of solder joints.

27. The system of claim 26, further comprising:
means for analyzing the plurality of error values to identify solder joint defects.

28. The system of claim 27, wherein the means for analyzing comprises a box
plot.

1 29. The system of claim 26, wherein the means for measuring comprises an
2 automated X-ray inspection system.

1 30. The system of claim 26, wherein the means for measuring comprises an optical
2 inspection system.

1 31. A solder-joint defect analysis detection program stored on a computer-readable
2 medium, comprising:

3 logic configured to record at least one characteristic of a plurality of solder joints on a
4 printed-circuit device;

5 logic configured to determine an expected value for the at least one characteristic for
6 the plurality of solder joints responsive to low frequency change in a solder joint
7 characteristics across the device;

8 logic configured to generate an error value from a mathematical combination of the
9 expected value and the recorded characteristic for the plurality of solder joints on the printed-
10 circuit device; and

11 logic configured to identify error value outliers.

12 32. The program of claim 31, wherein the logic configured to record records at
2 least one characteristic of a solder joint associated with an array package.

1 33. The program of claim 31, wherein the logic configured to determine an
2 expected value reflects a statistical analysis of the recorded characteristic.

1 34. The program of claim 31, wherein the statistical analysis comprises calculating
2 a median.

1 35. The program of claim 31, wherein the logic configured to generate an error
2 value calculates the difference of the recorded characteristic and the expected value.

1 36. The program of claim 31, wherein the logic configured to identify error value
2 outliers comprises a box plot analysis.

37. The program of claim 36, wherein the box plot analysis identifies error values that exceed a constant multiple of the interquartile range for the error values above a constant percentage of the error value data range.

38. The method of claim 1, wherein the step of obtaining comprises measuring the distance between a mounting surface of the printed-circuit device and a printed-circuit at a plurality of locations.

39. The method of claim 1, wherein the step of acquiring location information comprises an investigation of a quad flat pack package.

40. The method of claim 1, wherein the step of recording comprises a two-dimensional measurement.

41. The method of claim 1, wherein the step of recording comprises a three-dimensional measurement.

42. The method of claim 14, wherein the step of recording comprises an investigation of a quad flat pack package.

43. The method of claim 14, wherein the step of recording comprises a one-dimensional measurement.

44. The method of claim 14, wherein the step of recording comprises a two-dimensional measurement.

45. The method of claim 14, wherein the step of recording comprises a three-dimensional measurement.

46. The method of claim 1, wherein the step of estimating an expected value for a plurality of solder joints comprises performing a statistical analysis on the recorded measurements of a set of solder joints equidistant from the centroid of the printed-circuit device.

1 47. The program of claim 32, wherein the logic configured to estimate, estimates
2 responsive to the distance between the mounting surface of a printed-circuit device and a
3 printed-circuit board.

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